Notice of Referenc s Cited

Application/Control No. 10/040,953	Applicant(s)/Patent Under Reexamination TEIG ET AL.
Examiner	Art Unit
Andrea Liu	2825 Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Namê	Classification
	Α	US-			
	В	US-			
	C.	US-	تأمست ويبيه		
	Ď	US-		and the first of the second of	and the second state of the Same
	Ε	US-	4		v
	F	US-			
	G	US-	ران د داده ایت کست		
	H	US-	are reason of grants		
	: L	US-	e general		
	J	ÚS-			La Caracteria de la companya della companya della companya de la companya della c
	Κ,	US-			
	L	UŠ-		Manual Control of the	
	M	UŜ-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	Ň			10/2		
	0	talenda kanamanan arinda kanaman arinda kanaman arinda kanaman arinda kanaman arinda kanaman arinda kanaman ar	to accompany to			
	P	and the control of th		The state of the s		
	Q					
	R					30 - V
	S	man saa maa				
	Т		ا الله الله الله الله الله الله الله ال			

NON-PATENT DOCUMENTS.

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
×	U.	Resolving horizontal constraints and minimizing net wire length for multi-layer channel routing Pal, R.K.; Datta, A.K.; Pal, S.P.; Pal, A.;TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering. 1993 IEEE Region 10 Conference
X	V	Hierarchical physical design system Schulz, U., CompEuro '89., 'VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks', Proceedings., 8-12 May 1989
*	W	On the integration of partitioning and global routing for rectilinear placement problems Chingwei Yeh; Chi-Shong Wang; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 15 , Issue: 1 , Jan. 1996
×	х	Timing-driven hierarchical global routing with wire-sizing and buffer-insertion for VLSI with multi-routing-layer Deguchi, T.; Koide, T.; Wakabayashi, S.; Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific, 25-28

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Applicant(s)/Patent Under Application/Control No. Reexamination 10/040,953 TEIG ET AL. Notic of Referenc s Cited Art Unit Examiner Page 1 of 1 2825 Andrea Liu

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
-	Α	US-			
	, В .	US-			
	С	US-			
,	D	US-			
-	Е	US-			
	F	US-	·		
	G	US-			
	Н	US-			the second second
	1	US-::: 2': 2			
	J	US-			
	K	US-		3	
	L	US-	ر. دارند دراند دراند		
	M.	.US-	: **:		, A

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	and the second s	- 27			,
	, Ó	and the same of th				
	Р	A comment of the comm		11 -		
	Q					. ×
	R					
k	s				The second control of	
- 42	Ť.	and the second s			*	

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
X	·U	Resolving horizontal constraints and minimizing net wire length for multi-layer channel routing Pal, R.K.; Dátta, A.K.; Pal, S.P.; Pal, A.;TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering. 1993 IEEE Region 10 Conference
*	v	Hierarchical physical design system Schulz, U., CompEuro '89., 'VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks', Proceedings., 8-12 May 1989
¥	w	On the integration of partitioning and global routing for rectilinear placement problems Chingwei Yeh; Chi-Shong Wang; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 15 , Issue: 1 , Jan. 1996
X	х	Timing-driven hierarchical global routing with wire-sizing and buffer-insertion for VLSI with multi-routing-layer Deguchi, T.; Koide, T.; Wakabayashi, S.; Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific, 25-28

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.